STDN BPSK Demodulator

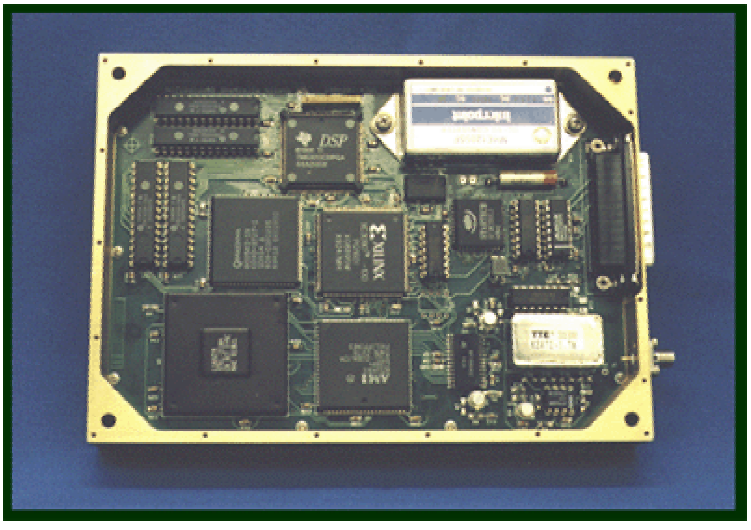
Features

* Utilizes digital ASIC technology to implement an all-digital demodulator.
* Coherent demodulation of up to 16-kbps BPSK signals modulated onto a subcarrier up to 1.7-MHz. It is compatible with the NASA STDN and Air Force SGLS standards.
* Bi-ϕ-L and NRZ-L signaling formats.
* BER performance within 1.5-dB of theoretical over an Eb/No of 2- to 12-dB.
* Power dissipation < 5 W. Single 28-V supply.
* Frame synchronization algorithm implemented internally.
* Balanced outputs drive 75-Ω loads compatible with EIA Standards RS-485 and RS-422A.
* Operating temperature range from -20°C to +70°C.
* All digital parameters are reconfigurable on the fly via an RS232 interface.

Functional Description

The SMC DMBP1700M-16K utilizes state-of-the-art digital ASIC technology to implement an all digital subcarrier demodulator (SCDM), compatible with the NASA STDN and Air Force SGLS standards. The input to the unit is a 16-kbps BPSK signal modulating a 1.7-MHz carrier.

A block diagram of the demodulator is shown in Figure 1. A 64-kHz bandpass filter limits the noise bandwidth at the front end, thus maximizing the Analog-to-Digital Converter (ADC) dynamic range. The digital components operate at an 8-MHz clock rate, well in excess of the Nyquist requirements. The digital downconverter translates the received digitized signal to baseband. The bit synchronizer provides a feedback signal to the digital downconverter for coherent carrier tracking. It also provides clock recovery and data alignment.



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A TMS320C30 Digital Signal Processor (DSP) processes the recovered bit stream. This includes implementation of the frame-synchronization algorithm shown in Figure 2. It monitors the downconversion feedback process to determine when phase lock has occurred. Bit-synchronizer information is monitored to determine when bit synchronization has occurred. TTL diagnostic signals are provided for external monitoring of the entire acquisition process.

The raw baseband-data and bit-sync-data are provided as test outputs for monitoring BER performance in the NRZ-L mode.

Operational parameters and modes are programmed vias an RS-232 interface to an IBM-compatible PC. In the Bi-ϕ-L mode, clock ambiguity is resolved in the DSP, soft decision information is stored over both halves of the 32-kbps effective bit interval and summed for hard decision. This restores the BER performance to that of 16-kbps NRZ-L data.

Frame Sync Algorithm

Frame synchronization follows the state diagram of Figure 2. The DSP is interrupt-driven by the bit-sync clock. Data is read into the processor, filling a 32-bit serial shift register, on the falling edge of each new bit (62.5 μs for NRZ-L mode). In the "search" mode, the processor watches for a positive or negative correlation with the 32-bit unique word. Positive correlation (PC) is defined as 2 or less disagreements between the data and unique word. Negative correlation is defined as 31 or more disagreements between the data and unique word (i.e. the carrier phase is off by 180$\tilde{}$°). If negative correlation is detected, all data is inverted from that point on; subsequently producing positive correlations.

Once correlation is achieved, the processor is placed in the "acquisition" state. Correlation is tested again after 8192 bits - the default frame length. If a PC is not achieved, the search state is re-entered. A PC causes the process to enter the "verify" state. Correlation is tested after another 8192 bits. If PC does not occur, the search state is re-entered. A PC here (3 correlations in a row) causes the state to enter the Lock Mode ("Lock 0" state). This is the normal operating state. Upon entering the Lock Mode, the data and clock outputs are activated, providing NRZ-L data. Any acceptable errors in the unique word (2 or less for a Hamming distance of 2) are corrected by the processor to minimize downstream correlation problems. The process continues in the Lock 0 state until a correlation failure is detected. If three consecutive correlation failures occur, the data and clock outputs are deactivated and the Search Mode is restarted.

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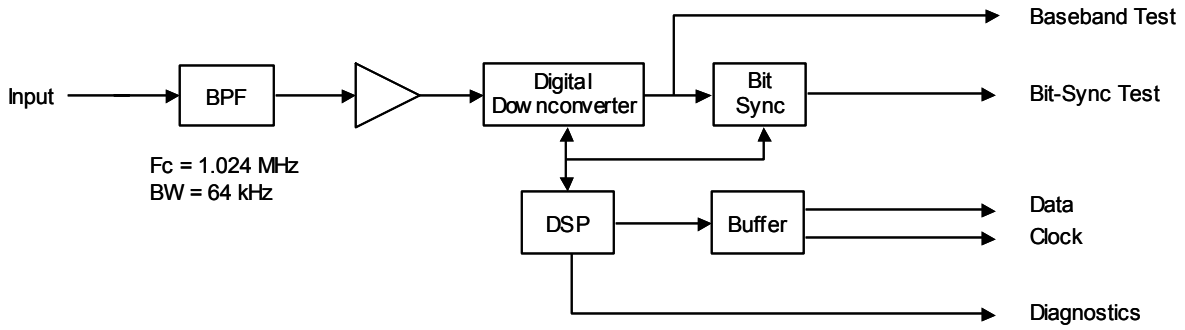

Figure 1 : SCDM Block Diagram

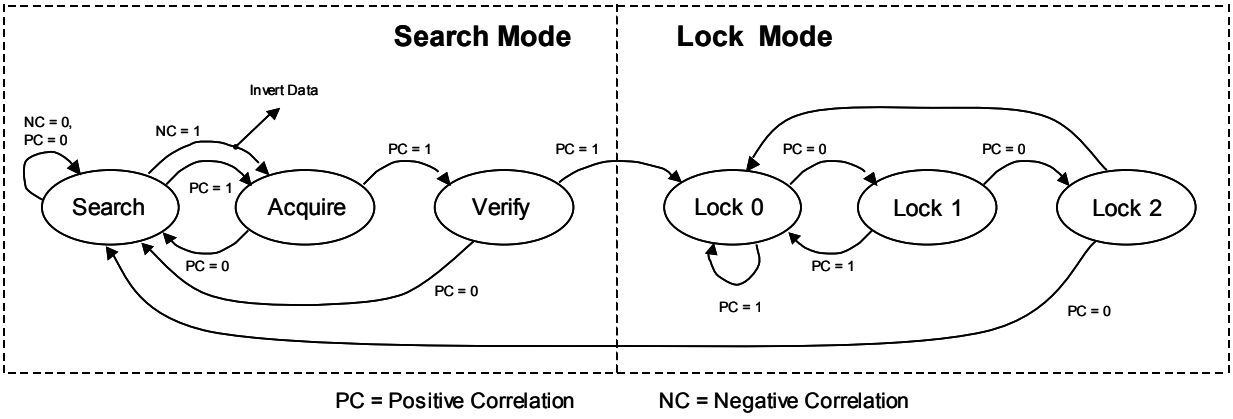

Figure 2 : State Diagram of Frame Sync Algorithm

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Electrical Interfaces

The following defines all interface lines and describes their application.

25-Pin D-Sub Connector (J1) :

The 25-pin D-Sub connector contains the main data and clock outputs and provides several diagnostic and test signals. Their definitions are as follows:

Pin 1 : NRZ-L Gated Data - This output pin provides the recovered data stream, capable of driving a 75-Ω load. It is only active when the demodulator is in the "frame-locked" mode. In Bi-ϕ-L operation, this output provides reconstructed NRZ-L data.

Pin 2 : NRZ-L Gated Data Return - This output provides the complement of Pin 1 and is capable of driving a 75-Ω load. Together, they comprise a balanced output compatible with EIA Standards RS-485 and RS-422A.

Pin 3 : NRZ-L Gated Clock - This output pin provides the recovered clock, capable of driving a 75-Ω load. It is only active when the demodulator is in the "frame-locked" mode. In Bi-ϕ-L operation, this output provides the reconstructed NRZ-L clock.

Pin 4 : NRZ-L Gated Clock Return - This output provides the complement of Pin 3 and is capable of driving a 75-Ω load. Together, they comprise a balanced output compatible with EIA Standards RS-485 and RS-422A.

Pin 5 : Phase Lock Indicator - This pin supplies a standard TTL high level when phase lock has been detected.

Pin 6 : Bit Sync Lock - This pin supplies a standard TTL "high" level when bit synchronization has been detected.

Pin 7 : Frame Sync Lock - This pin supplies a standard TTL "high" level when frame synchronization is detected.

Pin 8 : Ungated Bit-Sync Data - This output is a buffered version of the primary bit-synchronizer data output. It provides a standard TTL output level.

Pin 9 : Ungated Bit-Sync Clock - This output is a buffered version of the primary bit-synchronizer clock output. It provides a standard TTL output level.

Pin 10 : RS-232 Tx – Transmit line for the RS-232 interface.

Pin 11 : RS-232 Tx Rtn – Transmit return line for the RS-232 interface.

Pin 12 : RS-232 Rx – Receive line for the RS-232 interface.

Pin 13 : RS-232 Rx Rtn – Receive return line for the RS-232 interface.

Pin 14 : +15V – Primary positive input power.

Pin 15 : GND

Pin 16 : -15V – Primary negative input power.

Pin 17 : Frame-Sync Pulsed – TTL low during data output; high during frame-word output.

Pin 18 : Baseband Data – MSB of the I-Channel input to the bit-synchronizer.

Pin 19 : N/C

Pin 20 : Ungated Bit-Sync Data – Buffered TTL-level output of bit synchronizer data.

Pin 21 : Ungated Bit-Sync Clock – Buffered TTL-level output of bit synchronizer clock.

Pin 22 : GND

Pin 23 : GND

Pin 24 : GND

Pin 25 : GND

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Electrical Interfaces (cont)

Subcarrier Input (J2) :

The modulated signal is applied to the SCDM through this SMA connector. Input impedance is 75-Ω. The input carrier signal level is designed for 2.0 ± 0.4 V (peak-to-peak), regardless of noise-power spectral density.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	-54 to +85	˜ °C
T_a	Operating Temperature	-20 to +70	˜°C
V_{cc}	Supply Voltage	+18	V (max)
P_{in}	Signal Input Power	1	W (max) (75-□ load)

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Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
T_a	Operating Temperature	-20	-	+70	°C	
V_{cc}	Supply Voltage	+14	+15	+16	V	
I_{cc}	Supply Current	-	200	312	mA	frame sync achieved with data & clock driving 75-□ loads
V_{oh}	Pins 1- 4	3.0		5.0	V	driving 75-Ω loads
V_{ol}	Pins 1- 4	0.0		2.0	V	driving 75- Ω loads
V_{oh}	Pins 5-9, 17, 18, 20, 21	3.86		5.0	V	driving TTL loads
V_{ol}	Pins 5-9, 17, 18, 20, 21	0.0		0.4	V	driving TTL loads
V_{oh}	Pins 10-13	+5.0	+8.0	+15.0	V	driving RS232 3-K Ω loads
V_{ol}	Pins 10-13	-15.0	-8.0	-5.0	V	driving RS232 3-K Ω loads
V_{in}	Input Signal Level	1.6	2.0	2.4	V(p-p)	into 75- Ω load
F_{car}	Carrier Frequency	1.530	1.700	1.870	MHz	Min/Max based on loop BW
F_{mod}	Modulation Rate	15.68	16.0	16.32	kHz	Min/Max based on loop BW

Miscellaneous Electrical

The following specifications describe additional operational performance.

Bit-Sync Acquisition Time :
The probability of achieving bit synchronization within four seconds is ≥ 0.9 for Eb/No = 2- to 11-dB, and ≥ 0.99 for Eb/No > 12 dB.

Tracking Threshold :
Tracking threshold is defined as the Eb/No level at which the mean time to lose lock is no less than 10 seconds. The tracking threshold is Eb/No ≤ 5 dB.

Carrier Loop Bandwidth :
The AFC carrier-tracking-loop bandwidth is approximately 400 Hz. Since this loop is implemented using digital techniques, its value may be changed to accommodate a variety of user applications.

Bit-Sync Loop Bandwidth :
The bit-sync loop bandwidth is approximately 40 Hz. As with the carrier loop bandwidth, this value may be changed by selecting alternate digital constants.

BER Performance :
The bit error rate performance is within 1.5 dB of theoretical BPSK performance for Eb/No values in the range of +2- to +11-dB. Figure 3 presents measured BER performance for a typical unit over a range of Eb/No and temperature.

Frame Sync Pattern :
The frame synchronization pattern default is 1ACFFC1D (HEX); however, an alternate value may be reprogrammed via the RS232 interface.

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Environmental Performance

The following specifications define the environmental levels to which the SCDM is designed.

Temperature :

Operating : -20°C to +70°C
Non-Operating : -54°C to +85°C

Vibration :

6 g rms in the frequency range 20 Hz to 2000 Hz in any axis.

Shock :

Half sine wave shock of 50 g's for 11 ms duration in each of the three major axes.

Humidity :

95% relative humidity including condensation per MIL-STD-810.

Altitude :

Unlimited.

Mechanical Data

An outline drawing of the SCDM is shown in Figure 4. The design incorporates two multilayer printed circuit boards, back-to-back, separated by a module floor in the center of the housing. Proprietary design techniques are employed to assure good thermal conduction between the devices and the top and bottom metal surfaces. Mounting holes are available in each of the bottom corners.

Size: 5.0” x 7.0” x 1.0”

Weight: 1.5 lbs. (0.680 kg.)

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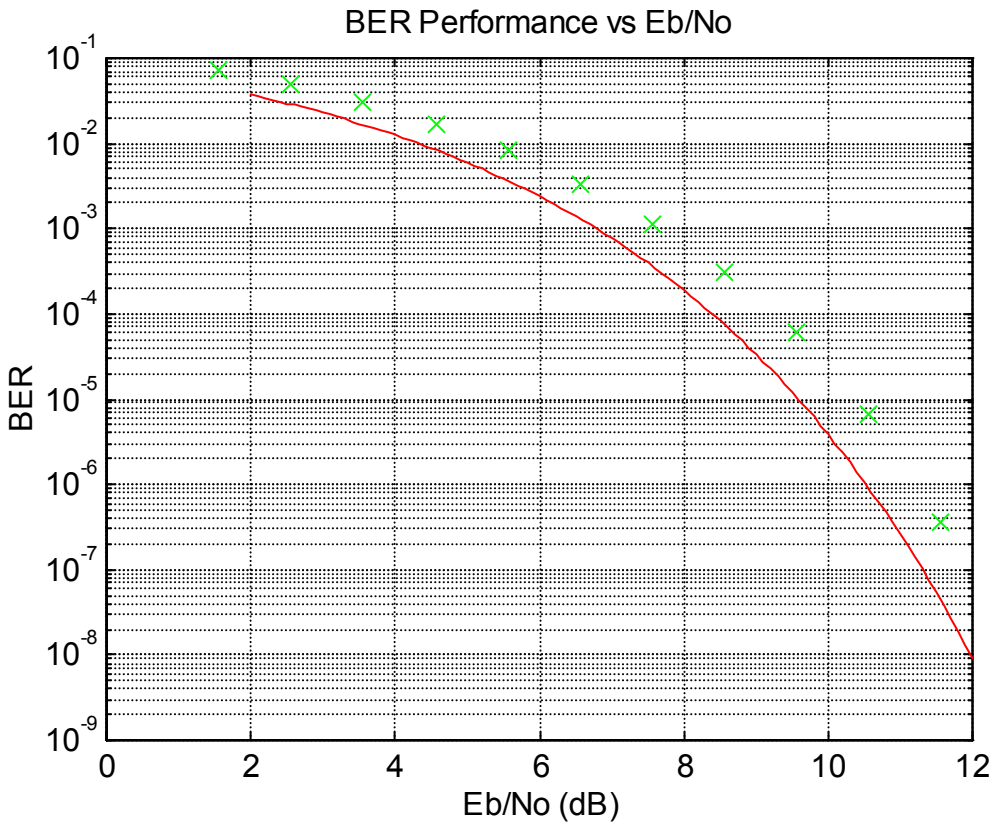

Figure 3 : Typical NRZ-L BER Performance

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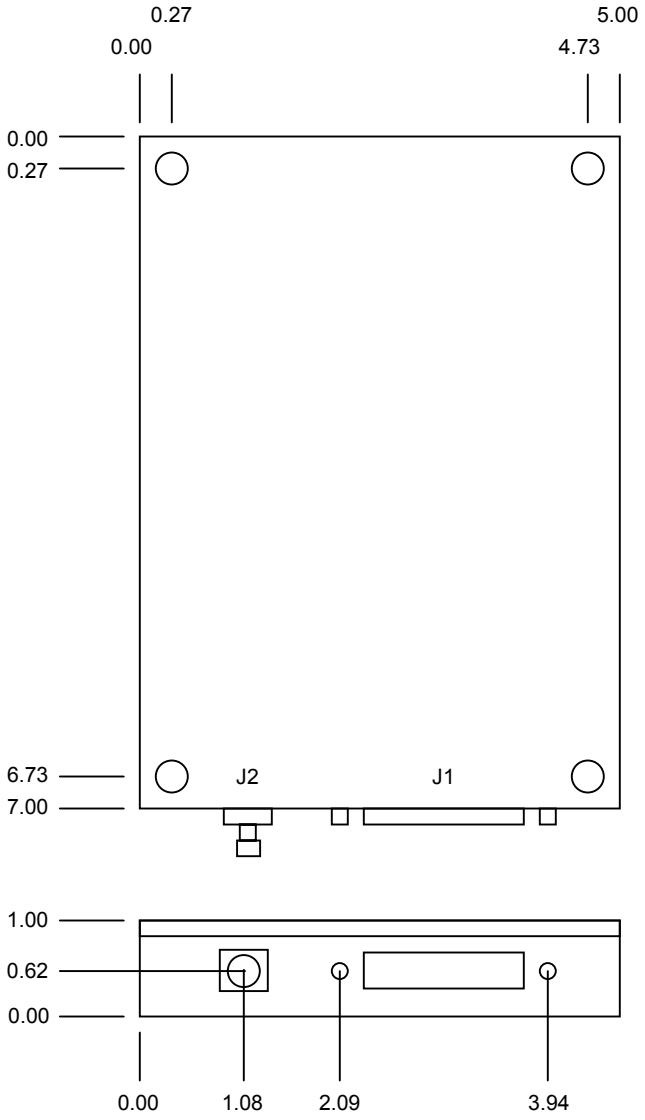

Figure 4 : Mechanical Outlines

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